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John D. Cressler,H. Alan Mantooth

Memory Systems Bruce Jacob, Spencer Ng, David Wang, 2010-07-28 Is your memory hierarchy stopping your microprocessor from performing at the high level it should be? *Memory Systems: Cache, DRAM, Disk* shows you how to resolve this problem. The book tells you everything you need to know about the logical design and operation, physical design and operation, performance characteristics and resulting design trade-offs, and the energy consumption of modern memory hierarchies. You learn how to tackle the challenging optimization problems that result from the side-effects that can appear at any point in the entire hierarchy. As a result you will be able to design and emulate the entire memory hierarchy. Understand all levels of the system hierarchy -Xcache, DRAM, and disk. Evaluate the system-level effects of all design choices. Model performance and energy consumption for each component in the memory hierarchy.

Cache and Memory Hierarchy Design Steven A. Przybylski, 1990 A widely read and authoritative book for hardware and software designers. This innovative book exposes the characteristics of performance-optimal single- and multi-level cache hierarchies by approaching the cache design process through the novel perspective of minimizing execution time.

PC Mag , 1992-02-11 PCMag.com is a leading authority on technology, delivering Labs-based, independent reviews of the latest products and services. Our expert industry analysis and practical solutions help you make better buying decisions and get more from technology.

DRAM Circuit Design Brent Keeth, R. Jacob Baker, Brian Johnson, Feng Lin, 2007-12-04 A modern, comprehensive introduction to DRAM for students and practicing chip designers Dynamic Random Access Memory (DRAM) technology has been one of the greatest driving forces in the advancement of solid-state technology. With its ability to produce high product volumes and low pricing, it forces solid-state memory manufacturers to work aggressively to cut costs while maintaining, if not increasing, their market share. As a result, the state of the art continues to advance owing to the tremendous pressure to get more memory chips from each silicon wafer, primarily through process scaling and clever design. From a team of engineers working in memory circuit design, *DRAM Circuit Design* gives students and practicing chip designers an easy-to-follow, yet thorough, introductory treatment of the subject. Focusing on the chip designer rather than the end user, this volume offers expanded, up-to-date coverage of DRAM circuit design by presenting both standard and high-speed implementations. Additionally, it explores a range of topics: the DRAM array, peripheral circuitry, global circuitry and considerations, voltage converters, synchronization in DRAMs, data path design, and power delivery. Additionally, this up-to-date and comprehensive book features topics in high-speed design and architecture and the ever-increasing speed requirements of memory circuits. The only book that covers the breadth and scope of the subject under one cover, *DRAM Circuit Design* is an invaluable introduction for students in courses on memory circuit design or advanced digital courses in VLSI or CMOS circuit design. It also serves as an essential, one-stop resource for academics, researchers, and practicing engineers.

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The Military Balance 2009 IISS, 2018-01-17 The Military Balance is The International Institute for Strategic Studies annual assessment of the military capabilities and defence economics of 170 countries worldwide. It is an essential resource for those involved in security policymaking, analysis and research.

The book is a region-by-region analysis of the major military and economic developments affecting defence and security policies, and the trade in weapons and other military equipment. Comprehensive tables detail major military training activities, UN and non-UN deployments, and give data on key equipment holdings and defence-expenditure trends over a ten year period. Key Features: Region-by-region analysis: major military issues affecting each region, changes in defence economics, weapons and other military equipment holdings and the trade in weapons and military equipment Comprehensive tables: key data on weapons and defence economics, such as comparisons of international defence expenditure and military manpower Analysis: significant military and economic developments Wallchart: detailed world map that shows current areas of conflict, with explanatory tables. This new edition of *The Military Balance* provides a unique compilation of data and information enabling the reader to access all required information from one single publication.

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Recent Advances in Intrusion Detection Robin Sommer,Davide Balzarotti,Gregor Maier,2011-09-01 This book constitutes the proceedings of the 14th International Symposium on Recent Advances in Intrusion Detection, RAID 2011, held in Menlo Park, CA, USA in September 2011. The 20 papers presented were carefully reviewed and selected from 87 submissions. The papers are organized in topical sections on application security; malware; anomaly detection; Web security and social networks; and sandboxing and embedded environments.

OpenMP in a New Era of Parallelism Rudi Eigenmann,Bronis R. Supinski,2008-04-25 OpenMP is a widely accepted, standard application programming interface (API) for high-level shared-memory parallel programming in Fortran, C, and C++. Since its introduction in 1997, OpenMP has gained support from most high-performance compiler and hardware vendors. Under the direction of the OpenMP Architecture Review Board (ARB), the OpenMP specification has evolved, including the recent release of Specification 3.0. Active research in OpenMP compilers, runtime systems, tools, and environments drives its evolution, including new features such as tasking. The community of OpenMP researchers and developers in academia and industry is united under cOMPunity (www.compunity.org). This organization has held workshops on OpenMP around the world since 1999: the European Workshop on OpenMP (EWOMP), the North American Workshop on OpenMP Applications and Tools (WOMPAT), and the Asian Workshop on OpenMP Experiences and Implementation (WOMPEI) attracted annual audiences from academia and industry. The International Workshop on OpenMP (IWOMP) consolidated these three workshop series into a single annual international event that rotates across the previous workshop sites. The first IWOMP meeting was held in 2005, in Eugene, Oregon, USA. IWOMP 2006 took place in Reims, France, and IWOMP 2007 in Beijing, China. Each workshop drew over 60 participants from research and industry throughout the world. IWOMP 2008 continued the series with technical papers, panels, tutorials, and OpenMP status reports. The first IWOMP workshop was organized under the auspices of cOMPunity.

Circuits and Systems for Security and Privacy Farhana Sheikh,Leonel Sousa,2017-12-19 *Circuits and Systems for Security and Privacy* begins by introducing the basic theoretical concepts and arithmetic used in algorithms for security and cryptography, and by reviewing the fundamental building blocks of cryptographic systems. It then analyzes the advantages and disadvantages of real-world implementations that not only optimize power, area, and throughput but also resist side-channel attacks. Merging the perspectives of experts from industry and academia, the book provides valuable insight and necessary

background for the design of security-aware circuits and systems as well as efficient accelerators used in security applications.

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Extreme Environment Electronics John D. Cressler, H. Alan Mantooth, 2017-12-19 Unfriendly to conventional electronic devices, circuits, and systems, extreme environments represent a serious challenge to designers and mission architects. The first truly comprehensive guide to this specialized field, *Extreme Environment Electronics* explains the essential aspects of designing and using devices, circuits, and electronic systems intended to operate in extreme environments, including across wide temperature ranges and in radiation-intense scenarios such as space. The Definitive Guide to Extreme Environment Electronics Featuring contributions by some of the world's foremost experts in extreme environment electronics, the book provides in-depth information on a wide array of topics. It begins by describing the extreme conditions and then delves into a description of suitable semiconductor technologies and the modeling of devices within those technologies. It also discusses reliability issues and failure mechanisms that readers need to be aware of, as well as best practices for the design of these electronics. Continuing beyond just the paper design of building blocks, the book rounds out coverage of the design realization process with verification techniques and chapters on electronic packaging for extreme environments. The final set of chapters describes actual chip-level designs for applications in energy and space exploration. Requiring only a basic background in electronics, the book combines theoretical and practical aspects in each self-contained chapter. Appendices supply additional background material. With its broad coverage and depth, and the expertise of the contributing authors, this is an invaluable reference for engineers, scientists, and technical managers, as well as researchers and graduate students. A hands-on resource, it explores what is required to successfully operate electronics in the most demanding conditions.

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Die-stacking Architecture Yuan Xie, Jishen Zhao, 2015-06-01 The emerging three-dimensional (3D) chip architectures, with their intrinsic capability of reducing the wire length, promise attractive solutions to reduce the delay of interconnects in future microprocessors. 3D memory stacking enables much higher memory bandwidth for future chip-multiprocessor design, mitigating the memory wall problem. In addition, heterogeneous integration enabled by 3D technology can also result in innovative designs for future microprocessors. This book first provides a brief introduction to this emerging technology, and then presents a variety of approaches to designing future 3D microprocessor systems, by leveraging the benefits of low latency, high bandwidth, and heterogeneous integration capability which are offered by 3D technology.

Multihomed Communication with SCTP (Stream Control Transmission Protocol) Victor C.M. Leung, Eduardo Parente Ribeiro, Alan Wagner, Janardhan Iyengar, 2012-12-19 Although multihomed communication is a rapidly emerging trend for next generation networks, no known book explores multihomed communication with the Stream Control Transmission Protocol (SCTP). Filling this void, *Multihomed Communication with SCTP (Stream Control*

Transmission Protocol) explains this innovative feature that allows an endpoint to sim

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Picture Archiving and Communication Systems (PACS) in Medicine K.S. Chuang,H.K. Huang,O. Ratib,A.R. Bakker,G. Witte,2013-06-29 This volume contains the proceedings of the NATO Advanced Study Institute on Picture Archiving and Communication Systems (PACS) in Medicine held in Evian, France, October 14- 26, 1990. The program committee of the institute consisted of H.K. Huang (Director), Osman Ratib, Albert Bakker, and Gerd Witte. This institute brought together approximately 90 participants from 15 countries. These proceedings are the accumulation of eight years of research and development results in PACS by various dedicated groups throughout the world. The purpose of this institute was to review the most recent technology available for PACS and some clinical results. The readers should notice the remarkable advances in this field by comparing the contents in these proceedings with those in a previous institute on Pictorial Information Systems in Medicine held August 27 - September 7, 1984 in Braunlage/Harz, Federal Republic of Germany, and published as Vol. 19 in this series. The institute was organized according to four categories: PACS components and system integration, PACS and related research in various countries and manufacturing companies, clinical experience and research support, and participants' scientific communications. In PACS components, we included image acquisition, workstations, data storage and networking. In system integration, topics on interfaces between Hospital Information System (HIS), Radiology Information System (RIS) and PACS, clinical reports, the ACR/NEMA standard, databases, reliability, and system integration were discussed. This lecture series emphasized the technical detail and how to aspects.

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